In the claims:

For the Examiner's convenience, all pending claims are presented below with changes shown in accordance with the new mandatory amendment format.

1-47. (cancelled)

48. (Previously Presented). A method comprising:

maintaining a first value for a first counter based on a content of a volatile memory;

maintaining a second value for a second counter based on a content of a non-volatile memory; and

controlling updates to the first value for the first counter and to the second value for the second counter, the first and second values used to generate a monotonic count.

49. (Previously Presented). The method of claim 48, wherein the controlling comprises updating the second value for the second counter when the first value for the first counter meets a predetermined condition.

50. (Previously Presented). The method of claim 48, comprising reading the first value for the first counter and the second value for the second counter, wherein the controlling comprises updating the first value for the first counter in response to the reading of the monotonic count.

51. (Previously Presented). The method of claim 48, wherein the controlling comprises updating the second value upon a power on reset.

52. (Previously Presented). The method of claim 48, wherein the controlling comprises updating the second value by programming a bit location or locations in a flash memory.

53. (Previously Presented). The method of claim 48, wherein the controlling comprises updating the second value by updating a portion of a flash memory when another portion of the flash memory meets a predetermined condition.

54. (Previously Presented). A method comprising:

reading a count value for a monotonic counter, the monotonic counter at least partially basing the count value on a content of a volatile memory and a non-volatile memory; and

updating the count value for the monotonic counter by utilizing contents of the volatile memory for lesser significant bits of the count value and contents of the non-volatile memory for higher significant bits of the count value.

55. (Previously Presented). The method of claim 54, wherein the updating the count value for the monotonic counter comprises updating a flash memory to update the non-volatile memory.

56. (Previously Presented). A method comprising:

powering on a monotonic counter, the monotonic counter at least partially basing a count value on a content of a volatile memory and a non-volatile memory; and

updating the count value for the monotonic counter on the powering on condition by utilizing contents of the volatile memory for lesser significant bits of the count value and contents of the non-volatile memory for higher significant bits of the count value.

57. (Previously Presented). The method of claim 56, wherein the updating the count value for the monotonic counter comprises updating a flash memory to update the non-volatile memory.

58. (Previously Presented). An apparatus comprising:

a volatile counter to maintain a first value;

a non-volatile counter to maintain a second value based on a content of a non-volatile memory; and

control logic to control updating the first and second values to control a monotonic count, the volatile counter to generate lesser significant bits of the monotonic count and the non-volatile counter to generate higher significant bits of the monotonic count.

59. (Previously Presented). The apparatus of claim 58, wherein the control logic controls the volatile counter to update the first value when the first and second values are read.

60.(Previously Presented). The apparatus of claim 58, wherein the control logic controls the non-volatile counter to update the second value when the volatile counter meets a predetermined condition.

61. (Previously Presented). The apparatus of claim 58, wherein the control logic controls the non-volatile counter to update the second value upon a power on reset.

62. (Previously Presented). The apparatus of claim 58, wherein the non-volatile memory comprises a flash memory and wherein the control logic to program a number of bit location or locations in the flash memory to update the second value.

63. (Previously Presented). The apparatus of claim 58, wherein the non-volatile memory is separated into more than one block of flash memory, wherein individual blocks of flash memory are arranged to provide cascading of selective number of the higher significant bits of the monotonic count.

64. (Previously Presented). An apparatus comprising:

a volatile memory to maintain a first value for a first counter;

a non-volatile memory to maintain a second value for a second counter; and

circuitry to maintain a count value for a monotonic counter, the circuitry to base the count value at least partially on the first value for lesser significant bits of the count

value and the second value for higher significant bits of the count value, and to update the count value by a number in response to a read of the count value for the monotonic counter.

65. (Previously Presented). The apparatus of claim 64, wherein the non-volatile memory comprises a flash memory and wherein the circuitry updates the count value by the number by programming a bit location or locations in the flash memory.

66. (Previously Presented). The apparatus of claim 64, wherein the non-volatile memory comprises a first block of flash memory and a second block of flash memory and wherein the circuitry updates the second block of flash memory and erases the first block of flash memory when a predetermined condition is met.

67. (Previously Presented). An apparatus comprising:

a volatile memory to maintain a first value for a first counter;

a non-volatile memory to maintain a second value for a second counter; and

circuitry to maintain a count value for a monotonic counter, the circuitry to base the count value at least partially on the first value for lesser significant bits of the count value and the second value for higher significant bits of the count value, and to update the count value by a number in response to a powering on condition for the circuitry.

68. (Previously Presented). The apparatus of claim 67, wherein the non-volatile memory comprises a flash memory and wherein the circuitry updates the count value by the number by programming a bit location of locations in the flash memory.

69. (Previously Presented). The apparatus of claim 67, wherein the non-volatile memory comprises a first block of flash memory and a second block of flash memory and wherein the circuitry updates the second block of flash memory and erases the first block of flash memory when a predetermined condition is met.

70. (Previously Presented). An apparatus comprising:

one or more registers to store a first value;

a first adder to maintain the first value;

a flash memory to store a portion of bits used for a monotonic count;

one or more registers to store a second value;

a second adder to maintain the second value based on one or more programmed locations in the flash memory; and

a control engine to control the flash memory and the first and second adders, the first value used to determine lower significant bits of the monotonic count and the second value used to determine higher significant bits of the monotonic count, the lesser significant bits being volatile while higher significant bits being non-volatile.

71. (Previously Presented). The apparatus of claim 70, wherein the second value is updated when a predetermined condition is met in the one or more registers storing the first value.

72. (Previously Presented). The apparatus of claim 70, wherein the second value is updated when a power on reset condition occurs.

73. (Previously Presented). A computer system comprising:

(a) a monotonic counter comprising:

(i) a volatile counter to maintain a first value,

(ii) a non-volatile counter to maintain a second value based on a content of a non-volatile memory, and

(iii) control logic to control updating the first and second values to control a monotonic count, the volatile counter to generate lesser significant bits of the monotonic count and the non-volatile counter to generate higher significant bits of the monotonic count; and

(b) one or more processors to read the first and second values.

74. (Previously Presented). The computer system of claim 73, wherein the control logic controls the volatile counter to update the first value when the first and second values are read.

75. (Previously Presented). The computer system of claim 73, wherein the control logic controls the non-volatile counter to update the second value when the volatile counter meets a predetermined condition.

76. (Previously Presented). The computer system of claim 73, wherein the control logic controls the non-volatile counter to update the second value upon a power on reset of the monotonic counter.